CLAIMS

1. An integrated circuit including a phase lock loop circuit comprising:

a clock input terminal for accepting a clock signal;

a phase/frequency detector (PFD) circuit including a reference clock input connected to the clock input terminal and including a PFD feedback input and including a PFD output;

a first charge pump (CP) circuit including a first CP input connected to the PFD output and including a first CP output;

at least one external feedforward output terminal connectable to couple at least one of a PFD output signal and a charge pump output signal to an external loop filter;

a loop filter (LF) including a filter input connected to the first CP output and including a LF output;

a loop controlled signal source (LCSS) including a LCSS input connected to the LF output and including a LCSS output; and

a feedback circuit connected between the LCSS output and the PFD feedback input, the feedback circuit including,

an external feedback input terminal;

first frequency selection circuitry including a first frequency selection input and including a first-frequency selection output and including counter circuitry programmable to produce on the output a first programmable feedback signal connectable to cause the LCSS to produce a LCSS output signal with a signal frequency that is a programmable multiple of a clock signal frequency received on the PFD clock input;

second frequency selection circuitry including a second frequency selection input and including a second frequency selection output and including second counter circuitry programmable to produce a second feedback signal on the second frequency selection output which is connectable to cause an external signal source to produce an external feedback signal with a frequency that is a programmable multiple of the clock signal received on the PFD clock input, wherein the second counter circuitry is connected so that during phase locking, there is a

dynamic adjustment of the number of external feedback signal input pulses received on the second frequency selection input that are required to produce each second feedback signal pulse on the second frequency selection output; and

multiplex circuitry connected with the LCSS output, the external feedback input terminal and the first and second frequency selection circuitry, the multiplex circuitry being operable to selectively couple one or the other of the LCSS signal and an external feedback signal to at least one of the first and second frequency selection inputs and so as to cause either the first programmable feedback signal on the first frequency selection output or the second programmable feedback signal on the second frequency selection output to be coupled to the PFD feedback input.

2. The integrated circuit of claim 1 wherein the first and second selection circuitry share at least one counter circuit.

3. The integrated circuit of claim 1 wherein the first and second frequency selection circuitry share at least one counter circuit that includes a counter output that serves as both the first frequency selection output and as the second frequency selection output.

4. The integrated circuit of claim 1 further including:

at least one external terminal connectable to couple an external loop filter signal to the LCSS.

5. The integrated circuit of claim 1 wherein the at least one feedforward terminal includes:

at least one terminal connected to the PFD output and includes at least one terminal connected to the CP output.

6. The integrated circuit of claim 1,

wherein the at least one feedforward terminal includes at least one terminal connected to the PFD output and includes at least one terminal connected to the CP output; and further including:

at least one external terminal connectable to couple an external loop filter signal to the LCSS.

7. The integrated circuit of claim 1 further including:

a second charge pump (CP) circuit including a second CP input connected to the PFD output and including a second CP output.

8. The integrated circuit of claim 1 further including,

a first external bias terminal; and

a second external bias terminal;

wherein the first charge pump is interconnected with the first and second external bias terminals.

9. The integrated circuit of claim 1,

wherein the second frequency selection circuitry includes counter circuitry connected to operate as an integer-N circuit.

10. The integrated circuit of claim 1,

wherein the second frequency selection circuitry includes counter circuitry connected to operate as a fractional-N circuit.

11. The integrated circuit of claim 1 further including:

a programmable reference counter connected to adjust the clock signal frequency and including an input connected to the clock input terminal and an output connected to provide the frequency adjusted clock signal to the PFD clock input.

12. The integrated circuit of claim 1 further including:

a second charge pump (CP) circuit including a second CP input connected to the PFD output and including a second CP output; and

wherein the second CP output serves as an external feedforward output terminal.

13. The integrated circuit of claim 1 wherein the at least one feedforward terminal includes:

at least one external PFD feedforward terminal connected to the PFD output and includes at least one external CP terminal connected to the first CP output; and further including:

selector circuitry connecting the PFD output to the at least one external PFD feedforward terminal and to the first CP input; and

selector circuitry connecting the first CP output to the at least one external CP feedforward terminal and to the LF.

14. The integrated circuit of claim 1 further including:

at least one external LF terminal connectable to couple an external loop filter signal to the LCSS.

selector circuitry connecting the LCSS to the LF output and to the external LF.

15. The integrated circuit of claim 1 further including:

a second charge pump (CP) circuit including a second CP input connected to the PFD output and including a second CP output;

an external second CP feedforward output terminal connected to the second CP output; and

selector circuitry connecting the PFD output to the first CP input and to the second CP input.

16. The integrated circuit of claim 1,

wherein the input of the first frequency selection circuit is connected to the LCSS output.

17. The integrated circuit of claim 1 further including:

driver circuitry connected to the clock input terminal.

18. The integrated circuit of claim 1 further including:

driver circuitry connected to the external feedback input terminal.

19. An integrated circuit including a phase lock loop circuit comprising:

a clock input terminal for accepting a clock signal;

a phase/frequency detector (PFD) circuit including a clock input connected to receive the clock signal and including a feedback input for receiving a PFD feedback signal and including a PFD output for providing a PFD output signal;

a first charge pump (CP) circuit including a first CP input connected to receive the PFD output signal and including a first CP output for providing a first CP output signal;

at least one external feedforward output terminal connectable to couple at least one of the PFD output signal and a CP output signal to an external loop filter;

a loop filter (LF) including a filter input connected to receive the first CP output signal and including a LF output for providing a LF output signal;

a loop controlled signal source (LCSS) including a LCSS input connected to receive a LF output signal and including a LCSS output for providing a LCSS output signal; and

a feedback circuit connected between the LCSS output and the PFD feedback input, the feedback circuit including,

an external feedback input terminal;

selector circuitry including a first feedback selection input connected to receive the LCSS output signal and including a second feedback selection input and including a selection output for providing a selection output signal;

a programmable program counter (PC) including a PC input connected to receive the selection input signal and including a PC output connected to provide a PFD feedback signal to the PFD feedback input;

a programmable swallow counter which includes a swallow counter input connected for receiving the PFD feedback signal and which includes a swallow counter output for providing a prescaler control signal; and

a programmable prescaler counter including a control input connected to receive the prescaler control signal and including a feedback input connected to receive a signal from the

external feedback input terminal and including a prescaler output connected to provide a prescaler signal to the second feedback selection input.

20. The integrated circuit of claim 19 further including:

a programmable reference counter connected to adjust the clock signal frequency and including an input connected to the clock input terminal and an output connected to provide the frequency adjusted clock signal to the PFD clock input.

21. The integrated circuit of claim 19,

wherein the selector circuit includes an other external feedback input; and further including:

a bypass connection between the external feedback input terminal and the other external feedback input of the selection circuit, the bypass connection bypassing the programmable prescaler counter.

22. The integrated circuit of claim 19 further including,

a first external bias terminal;

a second external bias terminal; and

a selector circuit connecting the first charge pump output to the LF and to an external feedforward output terminal; and

wherein the first CP is interconnected with the first and second external bias terminals;

23. The integrated circuit of claim 19 further including:

a second charge pump (CP) circuit including a second CP input connected to the PFD output and including a second CP output; and

wherein the second CP output serves as an external feedforward output terminal.

24. An integrated circuit including a phase lock loop circuit comprising:

a clock input terminal for accepting a clock signal;

a phase/frequency detector (PFD) circuit including a clock input connected to the clock input terminal and including a feedback input and including a PFD output;

a first charge pump (CP) circuit including a first CP input connected to the PFD output and including a first CP output;

a second charge pump (CP) circuit including a second CP input connected to the PFD output and including a second CP output;

an external feedback output terminal connected to the second charge pump output;

a loop filter (LF) including a filter input connected to the first CP output and including a LF output;

a loop controlled signal source (LCSS) including a LCSS input connected to the LF output and including a LCSS output; and

a feedback circuit connected between the LCSS output and the PFD phase detection input, the feedback circuit including,

an external feedback input terminal;

a counter circuit including a counter input connectable to multiply a frequency of the LCSS output by a programmable amount and to provide a resulting first programmable feedback signal to the PFD feedback input;

integer-N counter circuitry including a counter input connectable to the multiply frequency of an external feedback signal provided on the external input terminal by a programmable amount and to provide a resulting second programmable feedback signal on the PFD feedback input; and

selector circuitry connected to select either the counter circuit or the integer-N counter circuitry to provide a corresponding signal on the PFD feedback input.

25. A system including the integrated circuit of claim 1 further including:

an external loop filter (LF) and an external LCSS connected between the at least one external feedforward output terminal and the at least one external feedback input terminal.

26. A system including the integrated circuit of claim 1 further including:

at least one external LF input terminal connectable to couple an external loop filter signal to the LCSS

an external loop filter (LF) connected between the at least one external feedforward output terminal and the at least one external input LF terminal.